Code No.: 9A04605/R09

Set-2

B.Tech. III Year II Semester Regular & Supplementary Examinations

April/May - 2013

VLSI DESIGN

(Common to ECE, EIE and E.Con.E)

Time: 3 Hours | Max. Marks: 70

*Answer any **FIVE** Questions*

*All Questions carry **equal** marks*

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1. With neat sketches explain electron lithography process.

2. Explain clearly about different operating regions in nmos transistor with neat diagrams.

3. Draw the CMOS 2 input NAND gate, its physical layout with its stick diagram.

4. Estimate the total delay when a larger load capacitance is driven by a large inverter gate N which is driven by a small gate N-1 and so on.

5. (a) Provide the design of an 8 × 8 array multiplier.

   (b) Explain the working principle of booth multiplier.

6. (a) Write about standard cell based design.

   (b) Implement an optimized 3 × 8 binary decoder using PLA.

7. (a) What are the various styles of writing a program in VHDL? Explain.

   (b) Write a program using VHDL in structural style to implement a 3 × 8 binary decoder.

8. (a) What is a fault model? Explain in detail about stuck at fault model.

   (b) Explain the terms fault simulation, fault coverage and fault collapsing.